(12) UK Patent Application (19) GB (11) 2 243 948 (13) A

(43) Date of A publication 13.11.1991

(21) Application No 9021721.7

(22) Date of filing 05.10.1990

(30) Priority data
(31) 01105038 (32) 20.04.1990 (33) JP

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(51) INT CL[5]
H01L 29/784

(52) UK CL (Edition K)
H1K KCAL K1AA9 K1CA K4C11 K4C14 K4H1A K4H3A K4H3X K9D1 K9N2

(56) Documents cited
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US 4605947 A

(58) Field of search
UK CL (Edition K) H1K KCAL KHAA
INT CL[5] H01L
Online database: WPI.

(54) Field effect transistor

(57) A depletion type MOSFET has an undoped channel region and a gate electrode of a material having a smaller work function than that of the material of the channel region. Electrode materials comprise nitrides, carbides and LaB_6. An inverter comprising the depletion MOSFET of the invention together with an enhancement type MOSFET is described.

GB 2 243 948 A

FIG.1

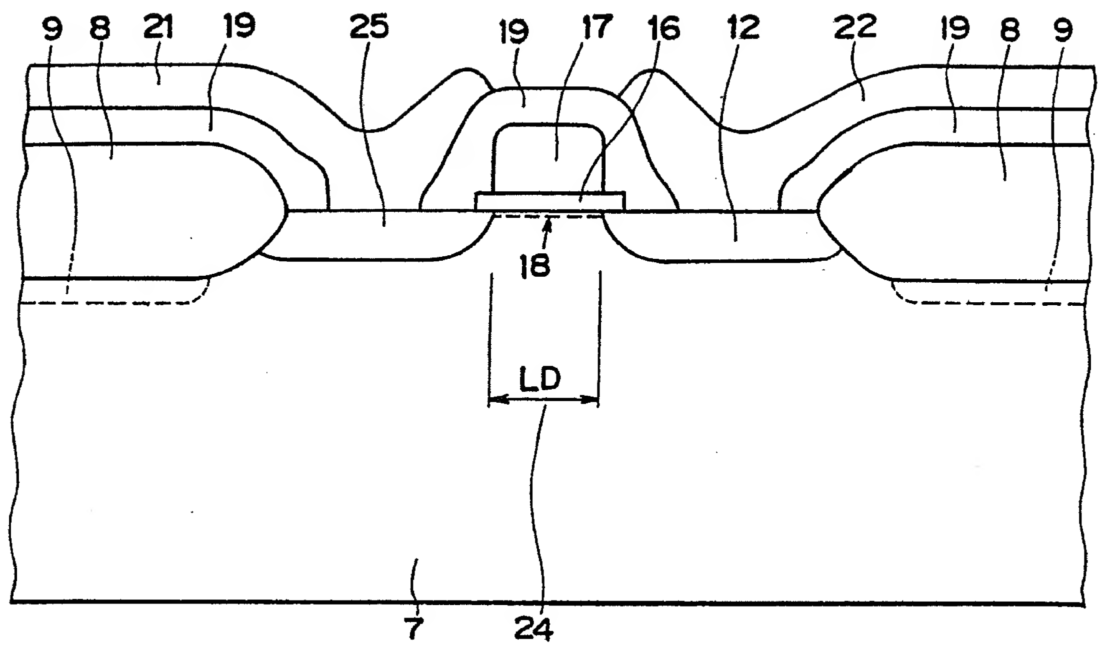

9
8
21
19
25
19
17
16
12
22
19
8
9
18
LD
7
24

FIG.2

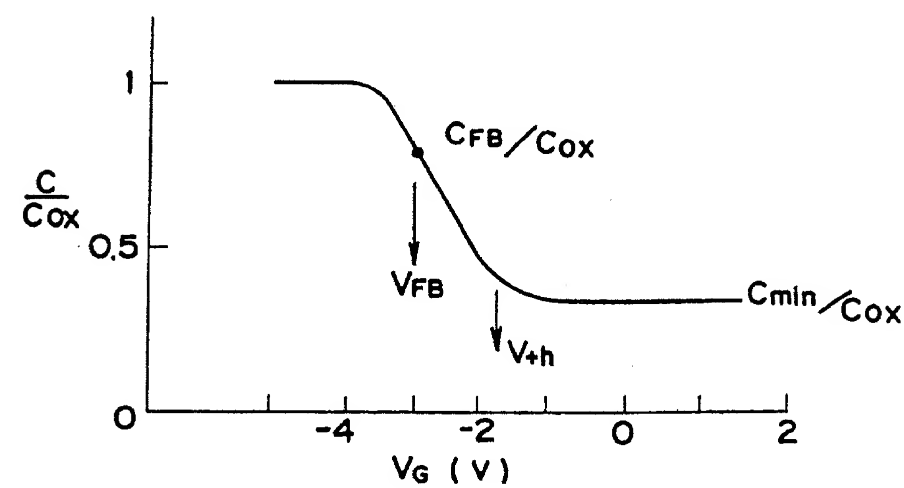

1
C/Cox
0.5
0
C_{FB}/C_{OX}
V_{FB}
V_{th}
Cmin/Cox
-4
-2
0
2
V_G (V)

FIG. 3A

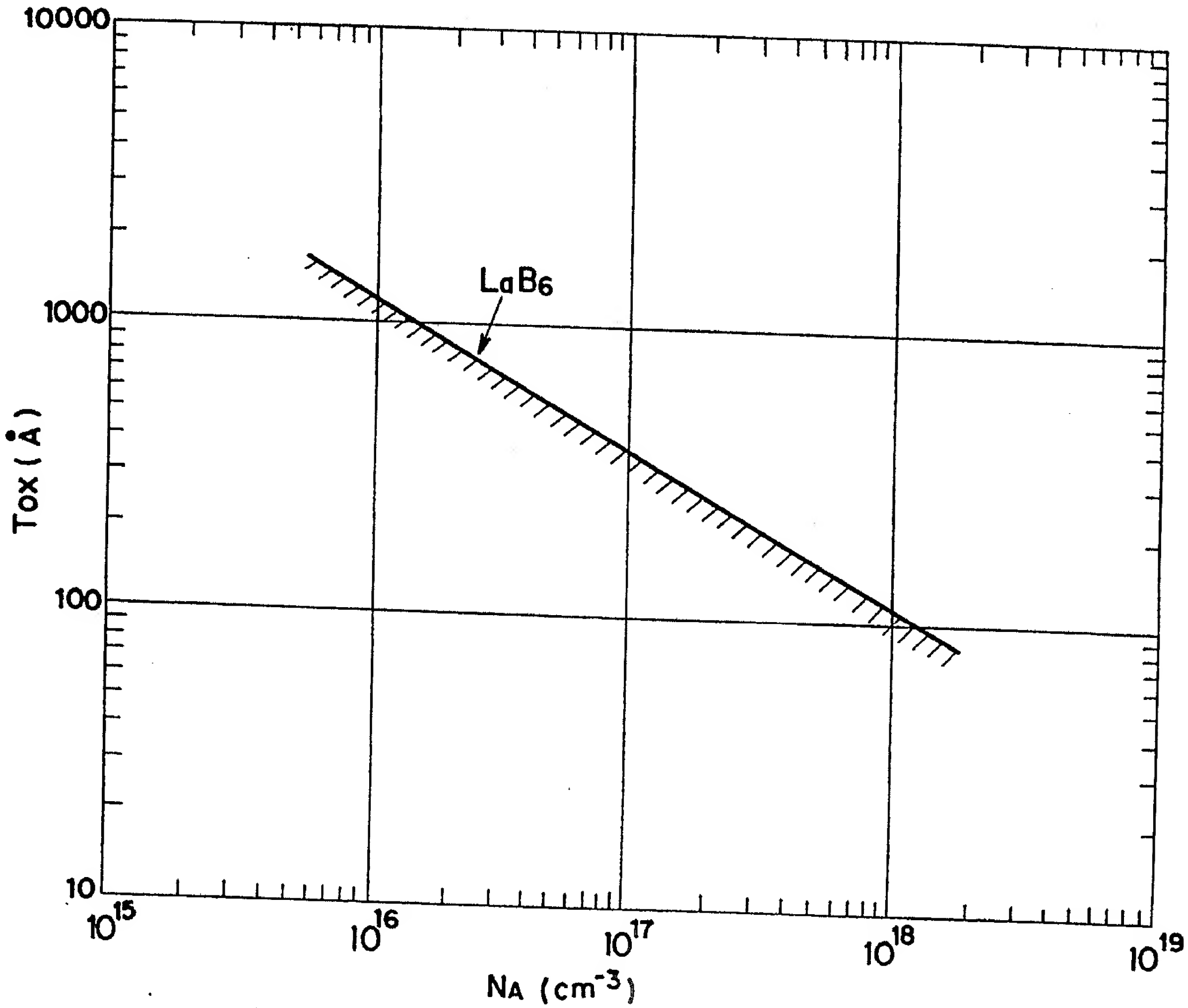
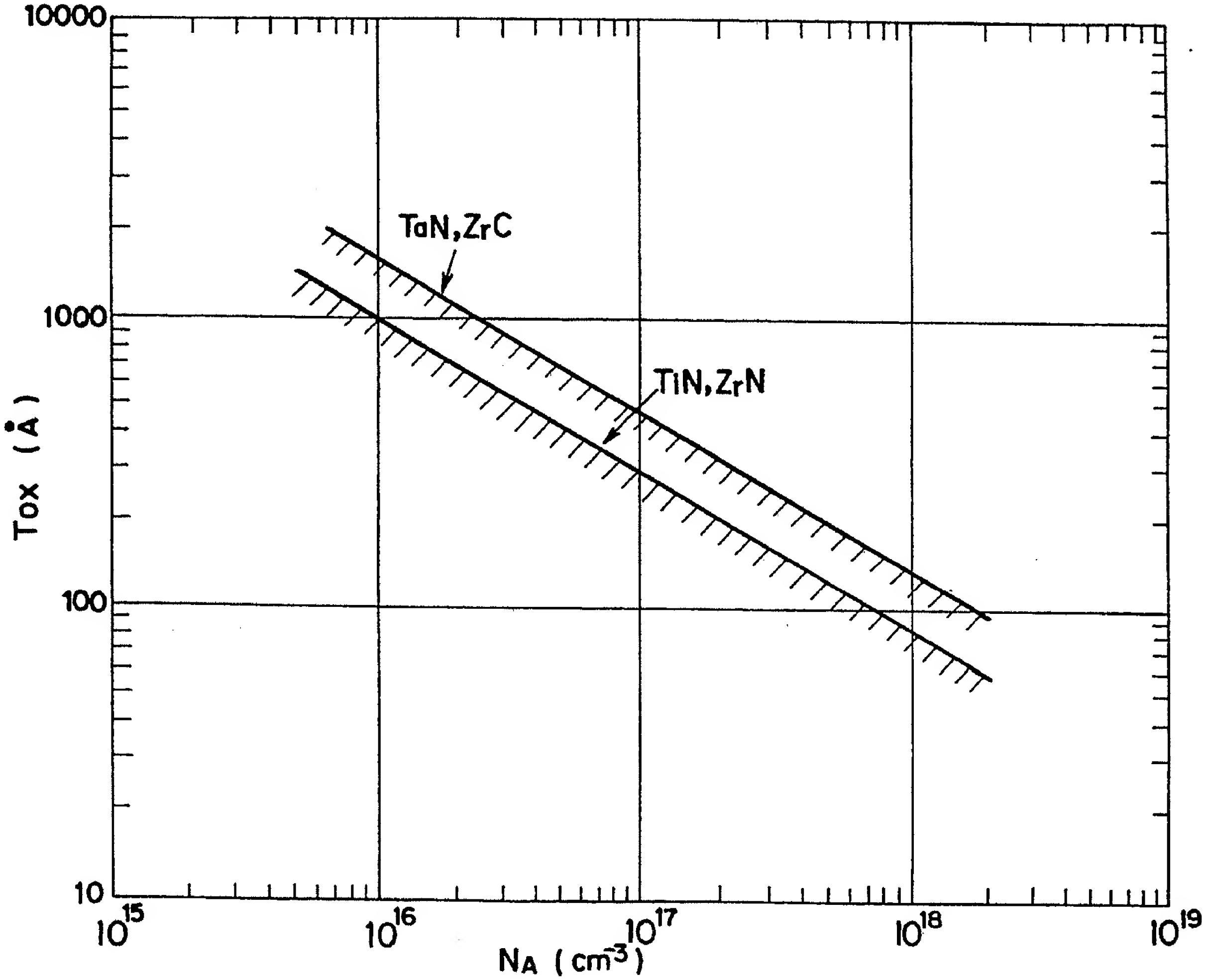


FIG. 3B



10000
1000
100
10
Tox (Å)
TaN, ZrC
TiN, ZrN
10^15
10^16
10^17
10^18
10^19
NA (cm^-3)

FIG. 4

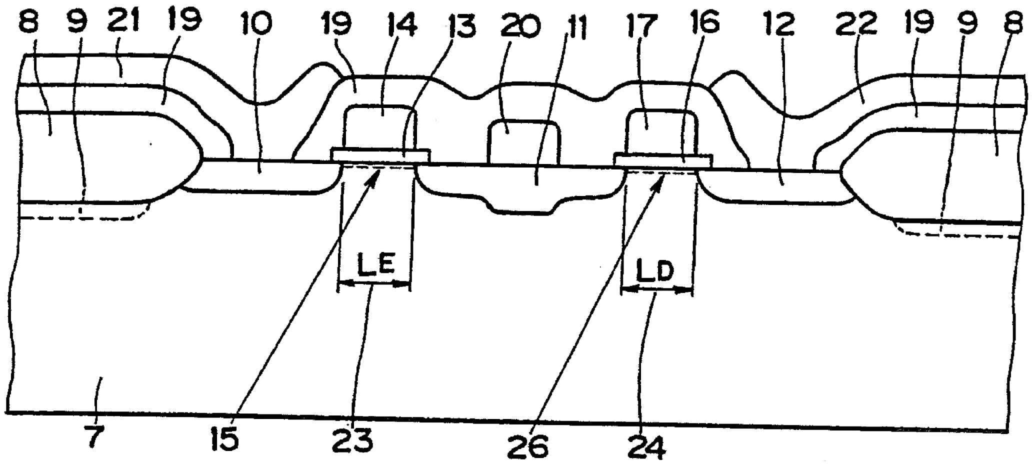


FIG. 5A

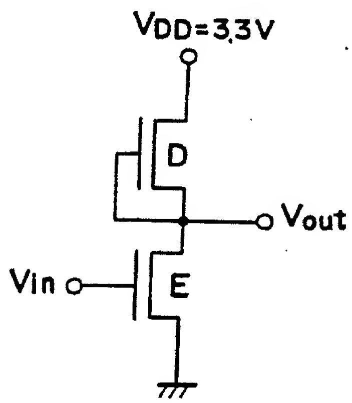


FIG. 5B

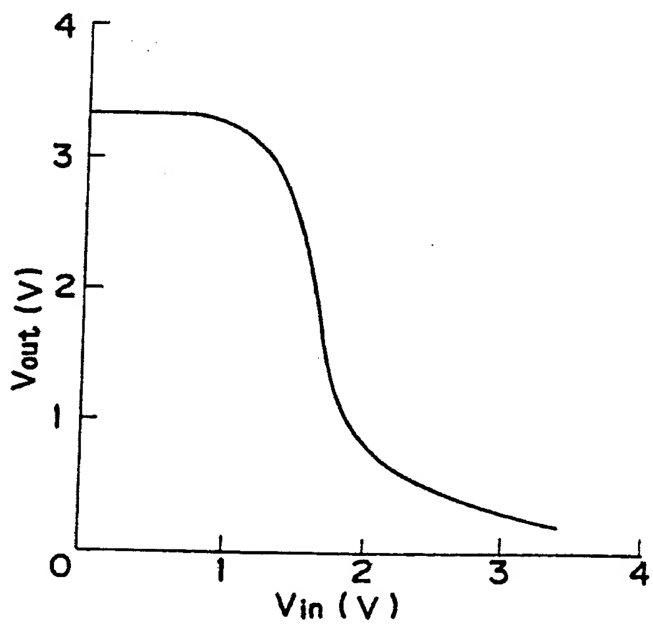


FIG. 6A

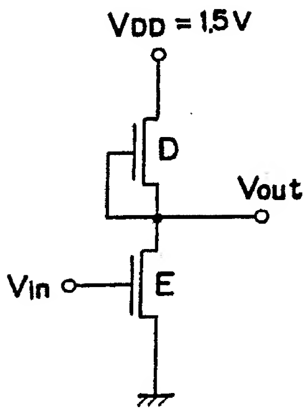


FIG. 6B

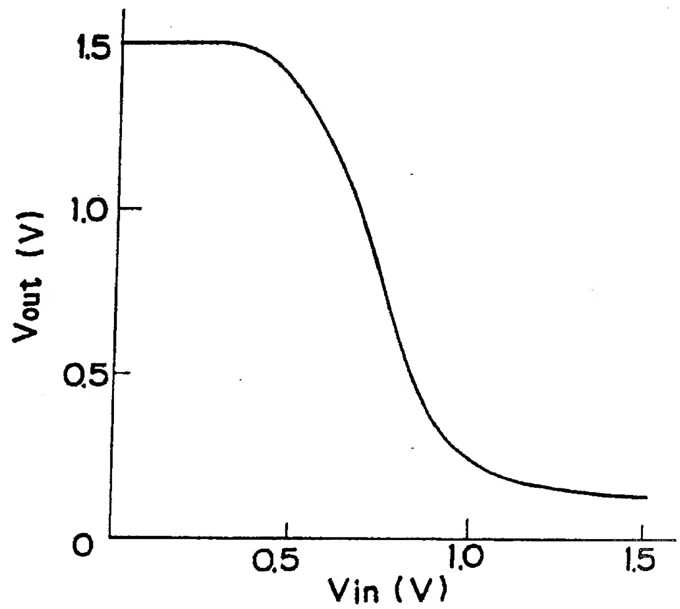


FIG. 7A

PRIOR ART

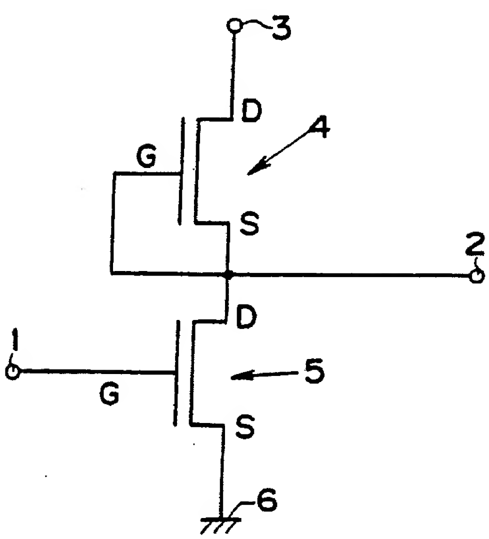


FIG. 7B

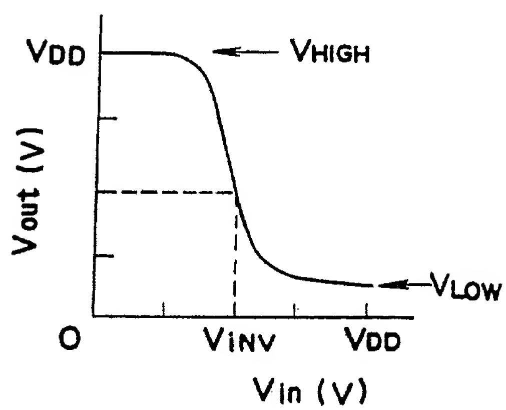


FIG. 8

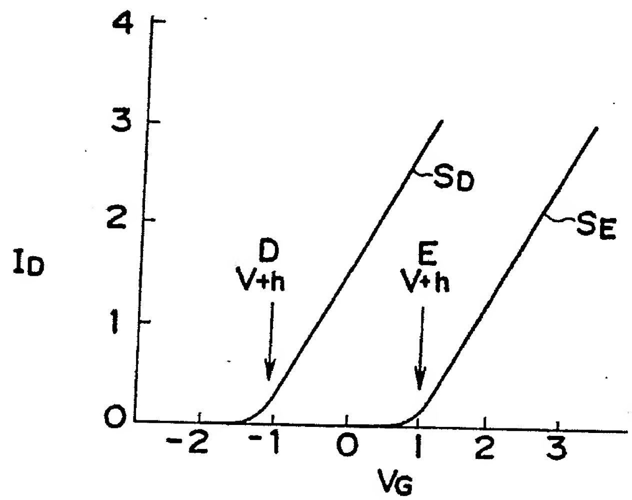


FIG. 9

PRIOR ART

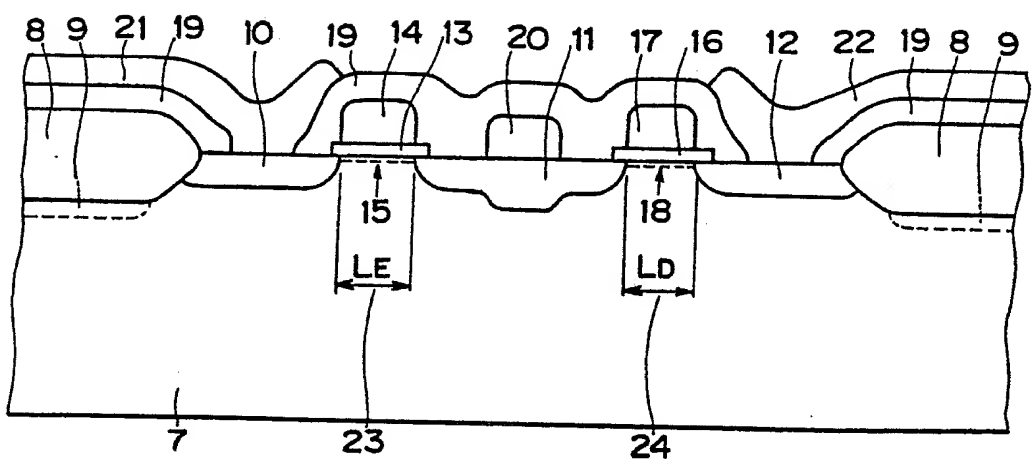


FIG.10

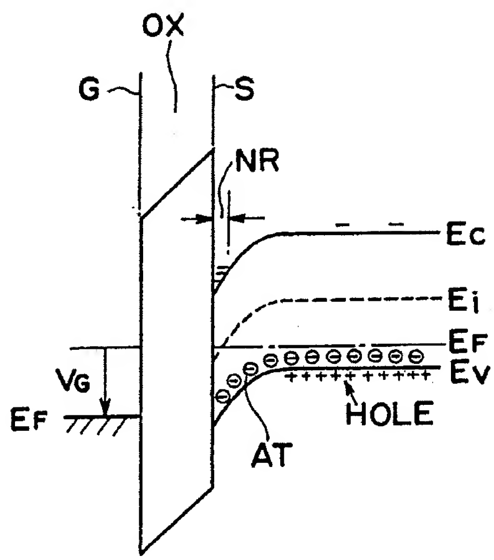


FIG.11

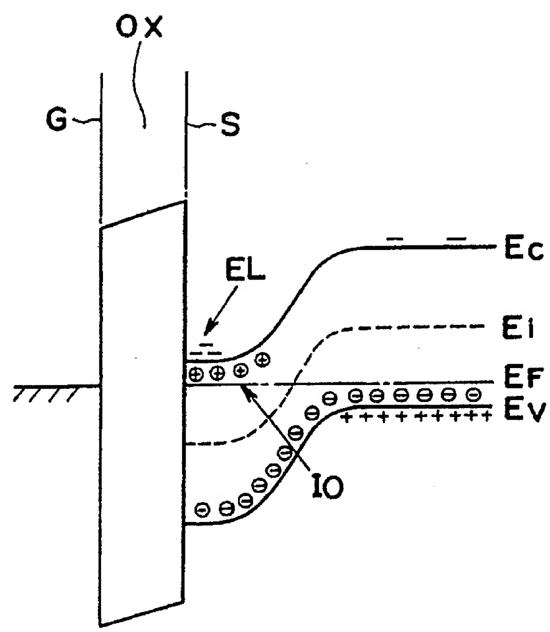


FIG. 12

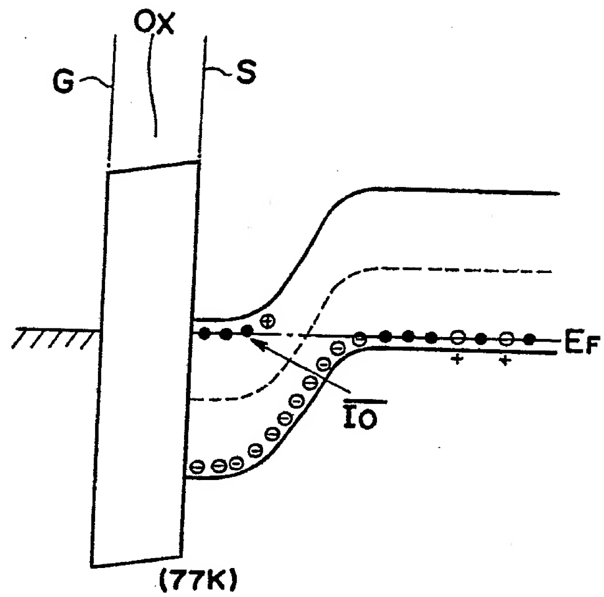
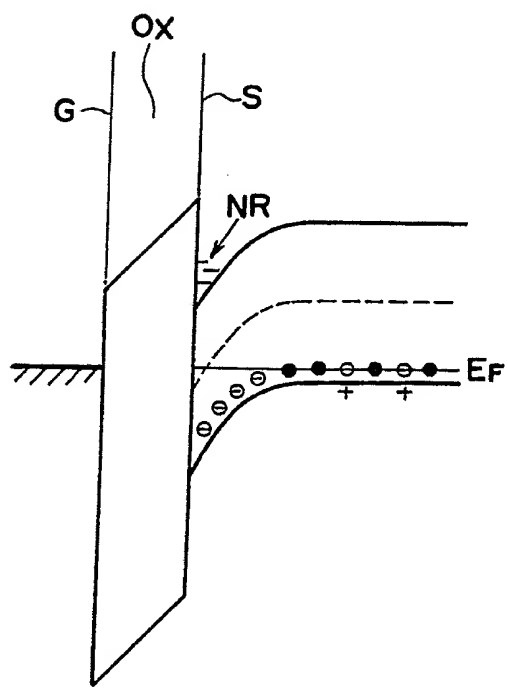


FIG. 13



INTEGRATED CIRCUIT

The present invention relates to an improvement of a depletion type field effect transistor (MOSFET) and in particular to an enhancement/depletion type inverter consisting of the FET stated above and an enhancement type FET and a semiconductor integrated circuit, in which these FETs or inverters are integrated on a substrate.

Increase in the speed and increase in the degree of integration of an integrated circuit using MOSFETs have been advanced, accompanied by the decrease in the size.

For example, contrarily to the fact that in a 1M D-RAM the smallest channel length is about 1.3μm, it is possible to realise an MOSFET having a channel length of about 0.1μm. Although the switching speed of a semiconductor logic circuit is increased together with the decrease in the size, it is said that the working speed thereof is generally lower than that of a logic integrated circuit using bipolar transistors. However the switching speed of the MOSFET increases due to the increase in the mobility and the saturation speed, if the working temperature is lowered from the room temperature (300K) to the liquid nitrogen temperature (77K). Further it is known that the RC time constant in the wiring is decreased by the decrease in the wiring resistance so that the working speed of the integrated circuit using MOSFETs can be as high as the working speed of the integrated circuit using bipolar transistors.

Even if a bipolar transistor is driven at the liquid nitrogen temperature, the switching speed thereof is not increased because of the freeze out in the base layer. Therefore it is difficult to increase the working speed of Si npn on pnp bipolar transistors having the prior art structure by low temperature operation.

It is known also that, since electric power consumption per gate for the MOSFET integrated circuit is smaller than that for the bipolar transistor integrated

circuit, the degree of integration per chip thereof is greater than that of the bipolar transistor integrated circuit. Thus, it can be expected to realise a high speed and high density LSI provided with both the high speed of the bipolar transistor LSI and a high degree of integration of the MOSFET LSI by driving an LSI using fine MOSFETs, whose channel length is smaller than than 1μm at liquid nitrogen temperature (77K).

Heretofore it was said that a Josephson logic circuit, working at liquid helium temperature (4.2K) as a low temperature device or integrated circuit, can realise a high speed logic integrated circuit. However, since a Josephson logic element utilising the superconduction phenomenon works only in the neighbourhood of 4.2K and it cannot work at room temperature, the operation thereof cannot be checked at room temperature. For example, in the case of constructing a large scale computer, it is not possible to rapidly exchange defective chips or boards and tremendous work and time are necessary. Therefore it is practically impossible to construct any large scale system. Consequently in a system, by which it is tried to obtain a high performance by a low temperature operation, it is necessary that the device or the system can be driven both at room temperature and at low temperature, although the working speed is low at the room temperature.

The MOSFETs can be driven essentially from room temperature to an extremely low temperature of 4.2K and therefore the construction of a large system by using them is easier than by using Josephson elements.

A prior art MOSFET integrated circuit driven at liquid nitrogen temperature is constructed by a complimentary type (CMOS) logic circuit, because the threshold voltage thereof does not vary significantly between the room temperature and 77K. However, since a logic circuit of enhancement/depletion structure (hereinbelow called D/D structure) can be constructed only

by n channel MOSFETs, the fabrication process therefor is easier than that for the CMOS logic circuit, for which it is required to integrate p channel MOSFETs and n channel MOSFETs on a same substrate. Further, since an NAND or NOR circuit having n inputs is constructed by 2n MOSFETs using the CMOS structure, contrarily to the fact that it is constructed by (n+1) MOSFETs by the E/D structure, in the case where a same logic circuit is constructed, the E/D structure has an advantage that it can be constructed by less MOSFETs than the CMOS structure.

Consequently, if a logic circuit of E/D structure can be constructed in such a small size that the channel length thereof is smaller than 0.5μm and driven stably both at room temperature and at liquid nitrogen temperature, a ultra-high speed ultra-high density integrated circuit provided with both the high speed of the bipolar transistor and the high density integration of the MOSFET can be realised by a relatively simple process, as described previously.

However, an MOSFET logic circuit of prior art E/D structure had the following problems and could not exhibit the characteristics described above.

Figure 7(A) shows an example of the prior art inverter circuit of E/D structure, in which reference numeral 1 is an input terminal; 2 is an output terminal; 3 is a source terminal; 4 is a depletion type n channel MOSFET: 5 is an enhancement type n channel MOSFET; and 6 is the ground. Since a logic integrated circuit or a memory integrated circuit is constructed by a modification of an inverter, such an inverter as described above is the basic unit of the integrated circuit. Since, in general, in Si the mobility of electrons is greater than the mobility of holes, n channel MOSFETs, by which a high speed operation is possible, are used. In the following explanation the case where n channel MOSFETs are used is taken as an example. Figure 7(B) shows an example of output characteristics of the inverter.

In the operation of the inverter circuit indicated in Figure 7(A), when the voltage in the input voltage V_{in} applied to the input terminal 1 is sufficiently lower than V_{INV}, a voltage, which is approximately equal to the source voltage V_{DD} applied to the source terminal 3, is produced at the output terminal 2. When a voltage, which is approximately equal to the source voltage V_{DD}, is applied as the input voltage V_{in}, the output voltage V_{out} has a level almost equal to zero. In practice the level is not at zero, but a slight voltage V_{LOW} is produced. Usually the voltage V_{LOW} is about 1/10 of the source voltage V_{DD}.

Concerning the characteristics S_E and S_D of the enhancement type n channel MOSFET and the depletion type n channel MOSFET, as indicated in Figure 8, the gate voltage (threshold voltage) V_{th}, by which the drain current I_D begins to flow, when the gate voltage V_G is applied, is positive (V_{th}^E) for the enhancement type and negative (V_{th}^D) for the depletion type.

In order to realise the inverter operation as indicated in Figure 7(B), the threshold voltage V_{th}^E and V_{th}^D of the enhancement type and the depletion type MOSFET constituting the inverter is designed so as to be about $0.2V_{DD}$ and $-0.6V_{DD}$, respectively. Figure 9 is a cross sectional view of an example of the MOSFET inverter of E/D structure indicated in Figure 7(A).

In the MOSFET indicated in Figure 9 the element isolation is effected by using the known LOCOS isolation method.

In the figure, reference numberal 7 is a p conductivity type Si substrate; 8 is a field oxide film; 9 is a p^+ doped region (channel stopper); 10 is an n^+ doped region (acting as the source region S of the enhancement type MOSFET); 11 is another n^+ doped region (acting as the drain region D of the enhancement type MOSFET and the source region S of the depletion type MOSFET formed in a same region); 12 is still another n^+

doped region (acting as the drain region D of the depletion type MOSFET); 13 is a gate insulating film for the enhancement type MOSFET; 14 is a gate electrode for the enhancement type MOSFET; 15 is a channel doped region of the enhancement type MOSFET doped with impurities of same conductivity as the p conductivity type Si; 16 and 17 are a gate oxide film and a gate electrode for the depletion type MOSFET, respectively; 18 is a channel doped region of the depletion type MOSFET doped with impurities of conductivity type opposite to the p conductivity type Si, 19 is a PSG film (insulating film); 20 is an electrode connected electrically with the gate electrode 16 for the depletion type MOSFET; 21 is an Aℓ metal wiring (ground line); 22 is an Aℓ metal wiring (source line); 23 represents the channel length of the enhancement type MOSFET; and 24 represents the channel length of the depletion type MOSFET.

The gate electrodes 14 and 17 are made of n^+ polycrystalline silicon. Ions of impurities such as B, etc. having the same conductivity type as the p conductivity type Si substrate 7 are implanted in the channel doped region 15 just below the gate oxide film 13 for the enhancement type MOSFET to adjust the threshold voltage V_{th}^E of the enhancement type MOSFET so as to be about $0.2V_{DD}$ with respect to the source voltage V_{DD}. P or As ions, which are impurities having the conductivity type opposite to the p conductivity type Si substrate 7 are implanted in the channel doped region 18 just below the gate oxide film 16 for the depletion type MOSFET to adjust the threshold voltage V_{th}^D of the depletion type MOSFET so as to be about $-0.6V_{DD}$ with respect to the source voltage V_{DD}.

The electrode 20 connected electrically with the gate electrode 17 for the depletion type MOSFET is extended in a plane perpendicular to the sheet. The electrode 20 is made of the same material as the gate electrode for the depletion type MOSFET, i.e. n^+

polycrystalline Si. The source of the depletion type MOSFET and the drain of the enhancement type MOSFET are connected with the n^+ region 11 through the electrode connected electrically with the gate electrode 17 for the depletion type MOSFET. The electrode 20 serves as the output terminal 2 of the inverter circuit indicated in Figure 7(A).

Figure 10 shows schematically the energy band in the part of gate electrode G/oxide film OX/p-Si; substrate S of an enhancement type MOSFET. The figure shows a case where a positive voltage is applied to the gate electrode and an n type inversion layer as well as ionized acceptor atoms AT are formed.

Since the enhancement type MOSFET forms an n type inverted layer in the surface portion of the Si substrate by being electrically the forbidden band in the surface portion of the p conductivity type Si substrate by the voltage applied to the gate electrode, both at the room temperature and at liquid nitrogen temperature it performs the enhancement type operation, i.e. the threshold voltage V_{th}^E remains positive.

Figure 11 shows schematically the energy band in the part of gate electrode G/oxide film OX/p-Si substrate S of a prior art depletion type MOSFET, in which ions such as P, As, etc., which are impurities of conductivity type opposite to that of the p conductivity type Si substrate, are implanted. At room temperature since there exist electrons EL due to ionization of As or P just below the gate oxide film, the MOSFET described above performs the depletion operation. In the figure IO indicates P or As atoms, with which the channel is doped, which are ionized at room temperature. However, at 77K, as indicated by 10 in Figure 12, since As or P implanted as opposite conductivity type impurities is frozen out and not ionized, in the case where no gate voltage is applied, no n channel layer is formed just below the gate oxide film 16 and therefore it does not perform the depletion

operation. That is, the MOSFET, which can perform the depletion operation owing to the implanted impurities of opposite conductivity type, performs the enhancement operation at the liquid nitrogen temperature.

Consequently, there was a problem that although the prior art inverter of E/D structure using depletion type MOSFETs including the channel portion 18 doped with the impurities of opposite conductivity type performs the normal operation at room temperature, it cannot perform the normal operation at liquid nitrogen temperature.

In the above explanation, no absolute value of the source voltage V_{DD} for the inverter on the MOSFET is dealt with. Heretofore the source voltage for the MOSFET was determined at 5V, in order to hold the interchangeability with TTL. However, if the source voltage is kept at 5V, for an MOSFET having a channel length smaller than 1μm, the electric field strength within the element is increased. Thus it has become more and more difficult to secure the normal operation and the reliability of the MOSFET because of hot carrier deterioration and drain break down. Consequently, the source voltage for the integrated circuit cannot help being decreased. For example, in the case of a channel length of 0.5μm, it is estimated to be about 3.3V and in the case of a channel length of 0.1μm, it is estimated to be about 1 to 1.5V.

Therefore, since in the high speed and high density MOSFET, the channel length is necessarily smaller than 1μm, the magnitude of the threshold voltage $V_{th}{}^{D}$ = 3.3V and about -0.6 to 0.9V when V_{DD} = 1 to 1.5V.

The MOSFET logic circuit of E/D structure is characterised in that the fabrication process is easier and the number of MOSFETs used for constructing a same logic circuit is smaller with respect to the logic circuit of CMOS structure.

The working speed of the logic circuits remains almost equal both for the E/D structure and for the CMOS structure and it is possible also therefor to increase the working speed by the operation at the liquid nitrogen temperature. However, as described previously, the inverter of E/D structure using depletion MOSFETs, in which the channel is doped with impurities of conductivity type opposite to the conductivity type of the used semiconductor substrate, has a drawback that it cannot perform the depletion operation at the low temperature because the impurities are frozen out at that time.

An object of an embodiment of the present invention is to provide an MOSFET capable of performing the depletion operation without doping the channel portion with impurities of conductivity type opposite to the conductivity type of the used semiconductor substrate and a method for constructing an inverter of E/D structure using it.

The present invention provides an integrated circuit including a depletion type field effect transistor comprising a first conductivity type semiconductor substrate; a source region formed on the principal surface side of said semiconductor substrate; a drain region formed in the neighbourhood of said source region on the principal surface side of said semiconductor substrate; a gate insulating film formed on the surface portion of said semiconductor substrate between said source region and said drain region which portion is not doped with an impurity of second conductivity type opposite to the first conductivity type; and a gate electrode formed on said gate insulating film comprising at least a layer of one of a group of materials comprising a nitride, a carbide and LaB_6 having a work function smaller than that of said first conductivity type semiconductor substrate and a further layer of one of a group of materials comprising polycrystalline silicon, a high melting point metal or silicide on any said layer of LaB_6.

Examples of the invention will now be described with reference to the drawings in which :

Figure 1 is a cross sectional view of an embodiment of the depletion type MOSFET, in which the channel portion is not doped with impurities of conductivity type opposite to the conductivity type of the substrate according to one embodiment of the present invention;

Figure 2 is a graph showing an example of measurements of the high frequency C-V curve for the depletion type MOSFET according to one embodiment of the present invention;

Figures 3A and 3B are diagrams showing the relation between the impurity concentration in the substrate, for which the threshold voltage is negative, and the thickness of the gate oxide film in the embodiment indicated in Figure 1.

Figure 4 is a cross sectional view of the n channel MOSFET inverter of E/D structure, for the depletion type MOSFET of which the channel is not doped with impurities of a conductivity type opposite to the conductivity type of the substrate.

Figure 5(A) is a circuit diagram of the E/D inverter according to one embodiment of the present invention;

Figure 5(B) is a graph showing an example of in/out characteristics of the E/D inverter indicated in Figure 5(A) for a channel length of 0.5μm;

Figure 6(A) is a circuit diagram of the E/D inverter according to another embodiment of the present invention;

Figure 6(B) is a graph showing an example of in/output characteristics of the E/D inverter indicated in Figure 6(A) for a channel length of 0.1μm;

Figure 7(A) is a circuit diagram of a prior art MOSFET inverter circuit of E/D structure;

Figure 7(B) is a graph showing an example of in/output characteristics of the prior art MOSFET inverter of E/D structure indicated in Figure 7(A).

Figure 8 is a graph showing an example of drain current (I_D) vs. gate voltage (V_G) characteristics of a prior art depletion type and a prior art enhancement type n channel MOSFET; and

Figure 9 is a cross sectional view of a prior art channel n MOSFET inverter of E/D structure, for the depletion type MOSFET of which the channel is doped with impurities of conductivity type opposite to the conductivity type of the substrate.

Figure 10 is a scheme of the energy band of the part of gate electrode/oxide film/p-Si in the enhancement type MOSFET;

Figure 11 is a scheme of the energy band of the part of gate electrode/oxide film/p-Si in the prior art depletion type MOSFET, in which the channel is doped with impurities of conductivity type opposite to the conductivity type of the substrate (300K);

Figure 12 is a scheme of the energy band of the same part as indicated in Figure 11, cooled at 77K; and

Figure 13 is a scheme of the energy band of the part of gate electrode/oxide film/p-Si, in the case where the gate electrode is made of a metal having a low work function.

If an MOSFET is constructed as described above, the forbidden band for the surface portion of the substrate is bent torwards the negative side by the difference in the work function in an energy band diagram using the electron energy. Therefore, although the surface portion is not doped with impurities of conductivity type opposite to that of the substrate, an n type inverted layer is formed in the surface portion of the substrate. Since the work function does almost not vary, depending on temperature, the n type inverted layer is formed in the surface portion of the substrate both at room temperature and at liquid nitrogen temperature.

Figure 13 shows a scheme of the energy band of the part of gate electrode/oxide film/p-Si in the depletion type MOSFET using a metal having a low work function. Since the energy band in the p conductivity type Si is bent by a difference in the work function between the gate electrode and the p-Si, an n type channel is formed just below the gate oxide film both at room temperature and at 77K, which makes the depletion operation possible.

Consequently the MOSFET constructed as described above can realise the depletion operation both at room temperature and at low temperature.

Further, when an E/D inverter is constructed, using a depletion type MOSFET constructed as described above and a prior art enhancement type MOSFET, it can perform the inverter operation both at room temperature and at liquid nitrogen temperature. In particular at low temperature it is possible to realise a logic circuit having a high switching speed owing to the increase in the mobility or the saturation speed.

Figure 1 is a cross sectional view of an embodiment of the depletion type MOSFET, in which the channel portion is not doped with impurities of conductivity type opposite to the conductivity type of the substrate.

In Figure 1, the same reference numerals as those used for Figure 9 represent identical or similar parts, and 25 is an n^+ doped region (the source region S of the depletion type MOSFET). The surface channel portion 18 of the Si substrate 17 just below the insulating film 16 for the gate electrode 17 is not doped with impurities of conductivity type (n type) opposite to the conductivity type of the substrate 7. This portion 18 may be doped with impurities of the same conductivity type (p type) as the substrate 7. Further the gate electrode 17 is made of a material having a work function, which is smaller than the work function of the p conductivity type Si substrate 7. The Si substrate 7 may be of n conductivity type. In this

case, the portion 18 described above is not doped with impurities of p conductivity type and the gate electrode 17 is made of a material having a work function greater than the work function of the substrate 7. Also in this case, the portion corresponding to the portion 18 stated above may be doped with impurities of same conductivity type as the n conductivity type substrate.

The basic structure is identical to that of an enhancement type n channel MOSFET fabricated by the LOCOS isolation method and the fabrication process therefor is identical to the well known n channel MOSFET process. The element isolation may be effected by any isolation method other than LOCOS isolation method e.g. the trench isolation method, if elements can be isolated thereby.

Further, although the structure indicated in Figure 1 corresponds to the well known SD (single drain) structure, it may correspond to the well known DD (double drain) structure on the LDD (lightly doped drain). What is essential is that the gate is made of a metal or a compound having a small work function.

One of the features of this example of the present invention is that the gate electrode is not made of n^+ type polycrystalline silicon, but a material having a small work function is used therefor. It is required for the material for the gate electrode to have a work function smaller than about 4eV.

The inventors of the present invention have found that although single metals La and Mg as well as LaB_6 in the form of a compound are preferable materials as concrete materials, LaB_6 is especially preferable, which has a high melting point and is chemically stable.

The melting point of LaB_6 is higher than 2000°C and bulk crystals thereof are used as a filament in an electron beam source. It is known that it is also chemically stable and has a low work function as bulk material.

The most undesirable elements in the Si MOSFET process are alkali metals producing movable ions in SiO_2. Further radioactive elements emitting x-ray are also undesirable elements. The inventors of the present invention have found that compound materials consisting of elements, which are widely used in the prior art Si process or in research and development and which are thought not to impair the reliability of Si LSI, can be used also as gate metal.

Si, Ge, B, P, As, W, Mo, Zr, Ta, Ti, Al, N, H, Ar, He, etc. can be cited as the elements, which don't impair the reliability of devices, etc. fabricated in the Si process. Among these elements, metals made of single elements have work functions higher than about 4eV and cannot be used as the low work function gate material for n channel MOSFETs. However, for example, if compounds such as nitride, a carbide, a silicide, etc. have a low work function, they can be used as the gate material. In general it is known that silicides have work functions higher than about 4eV. Therefore they are unsuitable for realising the present invention. Nitrides and carbites have high melting points and are chemically stable. Therefore, when they are introduced in the silicon process, they don't give rise to deteriorations in characteristics of fabricated MOS devices etc. However, the work functions of nitrides and carbides have been studied not in detail. Further, in the MOSFETs, since they are used in a thin film state, in order to know whether they can be applied to the gate metal having a low work function for the MOSFETs, it is necessary to fabricate an MOS diode or MOSFET in reality to verify whether the depletion operation thereof is possible.

The inventors of the present invention have found that LaB_6, nitrides and carbides, which are compounds having a high adaptability to the prior art Si process and giving rise to no deteriorations in characteristics, etc, can be used as the gate metal having a low work function.

As concrete materials LaB_6, nitrides such as TiN, ZrN, TaN, VN, etc., and carbides such as ZrC, TiC, TaC, HfC, etc., could be used as the gate metal having a low work function.

In particular, LaB_6, TiN, ZrN, TaN and ZrC have melting points higher than 1500°C and they are also chemically stable. Further TiN is used already as a barrier metal in the ohmic junction portion between Aℓ or Aℓ - Si also in MOSFET LSI, for which a high reliability of level for prodcuts in the market is required, and it is the material most suitable for depletion type MOSFETs giving rise to no deteriorations in characteristics.

Thin films of LaB_6, TiN, ZrN, TaN and ZrC can be formed by using the electron beam evaporation method, the sputtering method, the reactive sputtering method and the chemical vapor deposition method. All the thin films could be formed by the electron beam evaporation method. Further it was possible to form thin films of TiN, ZrN and TaN by the reactive sputtering method in an N_2 atmosphere, using targets made of Ti, Zr and Ta, respectively. Still further a TiN film could be formed by the chemical vapor deposition method, using Ti $(N(CH_3)_2)4$ and NH_3.

In the following embodiments LaB_6 was fabricated by using the well known electron beam evaporation method.

In the following embodiment TiN, ZrN, TaN and ZrC films were formed by the reactive sputtering method, by which the composition control was the easiest.

In a depletion type n channel MOSFET indicated in Figure 1 the channel portion just below the gate oxide film is not doped with impurities. In the case where the channel portion is doped with impurities having a conductivity type opposite to that of the substrate, the threshold voltage is changed at room temperature and 77K, because the impurities with which the channel is doped, are frozen out at 77K. On the other hand, in the case where the channel is doped with impurities having the

same conductivity type as the substrate, since they are not frozen out, the threshold voltage remains almost unchanged at room temperature and 77K.

For example, when the impurity concentration in the p conductivity type Si substrate was about $1x10^{16}cm^{-3}$, the gate oxide film was about 20mm thick and an LaB_6 gate electrode was used as the gate metal, the threshold voltage of the MOSFET was about -1.6V. On the other hand, e.g. when the impurity concentration in the p conductivity type Si substrate was about $1x10^{16}cm^{-3}$, the gate oxide film was about 20mm thick and TiN was used as the gate metal, the threshold voltage of the MOSFET was about -1.2V. When the channel was doped with impurities having the same conductivity type as the substrate, it was possible to vary the threshold voltage in the positive direction e.g. to 1.0V or -0.5V by increasing the amount of the channel dope.

Although in Figure 1 the gate metal is formed by one layer of e.g. LaB_6 or TiN, another layer made of polycrystalline Si, high melting point metal or silicide may be formed on the LaB_6 or TiN layer. The resistivity of the thin film made of LaB_6, TiN, ZrN, TaN or ZrC is as high as several tens or several hundreds of $\mu\Omega$cm. When a film made of a metal, whose sensitivity is several $\mu\Omega$cm, or a silicide whose sensitivity is 10 to several 10 $\mu\Omega$cm is formed on the film of LaB_6 TiN, ZrN, TaN or ZrC, the effective resistivity of the gate electrode was able to be effectively reduced. In the case where the material for the gate electrode is used as wiring metal, as it is, in a complicated logic circuit for the reason of the process, the gate structure of two or three layers is a desirable structure for low resistance wiring. What is essential is to form a material having a low work function just below the gate oxide film.

In the case of the MOSFET, the threshold voltage is shifted, depending on the interfacial fixed charge density. However, in the case of the n channel MOSFET,

since the threshold voltage increases in the negative direction, if the interfacial fixed charge density is high, it is never driven in the enhancement operation owing to the high interfacial fixed charge density.

As described above, although the threshold voltage is negative for the n channel MOSFET, for the inverter of E/D structure the magnitude of the threshold voltage is a problem. For the inverter of E/D structure, the threshold voltage V_{INV} of the inverter is defined as a voltage, for which the output voltage V_{out} is equal to the input voltage V_{in} in the inverter characteristics indicated in Figure 7(B). By a well known designing method the threshold voltage of the inverter is set at about $-0.6V_{DD}$ so that the switching speed remains approximately equal at the turning-on and the turning-off of the input voltage at about 1/2 of the source voltage V_{DD} of the inverter. Consequently, in the case where the source voltage V_{DD} is 5V, the threshold voltage of the depletion type MOSFET is about -3V.

In the ultra-high speed high density MOSFET logic circuit, since it is composed of fine MOSFETs, whose channel length is smaller than about 0.5μm, the threshold voltage is about 3.3V, when the channel length is about 0.5μm, and 1 to 1.5V, when it is about 0.1μm. Therefore the threshold voltage of the depletion type MOSFET should be set at about -2V, when the channel length is about 0.5μm, and -0.6 to -1.0V, when it is 0.1μm.

In a depletion MOSFET using LaB_6, TiN, ZrN, TaN or ZrC, the lower limit of the threshold voltage obtained, when the impurity concentration in the p conductivity type substrate was as low as e.g. $1x10^{15}cm^{-3}$ and the gate oxide film was as thin as about 5mm, was about -2V. Further, even if the thickness of the gate oxide film was constant, it was possible to control the gate voltage in a region from -2V to 0V by implanting B ions, etc., which are impurities having the same conductivity type as the p

conductivity type substrate, in the channel position. Consequently the depletion type MOSFET can be used for the inverter of E/D structure using fine MOSFETs, whose channel length is smaller than 0.5μm, in which the gate oxide film should be as thin as about 5 to 20nm and the source voltage should be as low as about 1 to 3.3V.

Figure 4 is a schematic cross sectional view of an inverter having the E/D structure using LaB_6 or TiN or ZrN or TaN or ZrN or TaN or ZrC for the gate metal.

In the figure, the reference numerals identical to those indicated in Figures 1, 5 and 9 represent idential or corresponding items and 26 is the channel portion of the depletion type MOSFET, which is not doped with impurities of conductivity type opposite to the conductivity type of the substrate.

As the fabrication process of the embodiment described above, the n MOS process using the well known LOCOS isolation technique was used. The isolation may be effected by using any method other than the LOCOS isolation method. It is required only to be able to isolate different elements. However, contrarily to the well known n MOS process, the part of the p conductivity type Si 26 just below the gate oxide film 16 in the depletion type n channel MOSFET is not doped by the ion implantation, etc. with impurities such as As and P having the opposite conductivity type. TiN or TaN or ZrN or ZrC was formed by using the reactive sputtering method. LaB_6 was formed by using the well known electron beam evaporation method. Although, in Figure 4, the gate metal is of one-layered structure made of TiN, etc., polycrystalline silicon, a high melting point metal, silicide, etc. may be formed on the layer made of TiN, etc. so that the gate electrode is of two or three-layered structure. What is essential is that LaB_6 or TiN or ZrN or TaN or ZrC which is a metal having a low work function, is formed directly on the oxide film. The source and drain region of the depletion type n channel MOSFET was

formed by implanting ions of P after the formation of the gate electrode.

Further, for the gate electrode 14 of the enhancement type MOSFET, the conventional n^+ polycrystalline Si was used.

The gate electrode of the enhancement type MOSFET may be not of one-layered structure made of n^+ type polycrystalline Si, but of polycide structure, in which a silicide layer is formed on the n^+ type polycrystalline layer. Further not n^+ type polycrystalline Si, but silicides of W, Ti, Ta, etc. may be used for the gate metal. High melting point metals such as Mo, W, etc. may be also used therefor. Furthermore, Aℓ may be used therefor.

In order to control the threshold voltage of the enhancement type MOSFET, ions of B, which are impurities of same conductivity type as the p conductivity type Si, were implanted in the channel portion before the formation of the gate oxide film 13, The ions of B were implanted so that the threshold votage V_{th}^E is about 0.7V for an MOSFET having a channel length of about 0.5μm and the threshold voltage V_{th}^E is about +0.3V for an MOSFET having a channel length of 0.1μm.

On the other hand, in order to control the threshold voltage of the depletion type MOSFET, ions of B, which are impurities of same conductivity type as the p conductivity type Si substrate, were implanted in the channel portion before the formation of the gate oxide film 2. The ions of B were implanted so that the threshold voltage V_{th}^E is about -1.5 to -2V for an MOSFET having a channel length of 0.5μm and the threshold V_{th}^D is about -1V for an MOSFET having a channel length of 0.1μm.

Although in the present embodiment impurities of same conductivity type as the p conductivity type Si were implanted for the control of the threshold voltage, the ion implantation is not necessarily effected, if the threshold voltages of the enhancement type MOSFET and the depletion type MOSFET are about $0.2V_{DD}$ and about $-0.6V_{DD}$, respectively, with respect to the source voltage V_{DD} of the E/D inverter.

If ions of P or As, which are impurities of conductivity type opposite to the p conductivity type Si, were implanted in the channel portion at the fabrication of the depletion type MOSFET according to the prior art technique, although an n type channel is formed, which performs the depletion type operation at room temperature, at liquid nitrogen temperature (77K), since P or As impurities are implanted as n conductivity type impurities would be exhausted, no n type channel layer would be formed and it would not perform the depletion type operation. However, in the case where the channel portion is doped with impurities of p conductivity type with respect to the p conductivity type Si only for the purpose of varying the concentration thereof, since they are not frozen out, the freeze out described previously has influences neither at room temperature nor at 77K. Therefore, the E/D inverter according to the present embodiment was able to perform the normal inverter operation both at room temperature and at 77K. Contrarily to the fact that the E/D inverter using conventional depletion type MOSFETs performed no normal operation at 77K, the E/D inverter performed the normal operation both at room temperature and at 77K.

A ring oscillator was constructed by connecting E/D inverters described above in a multi-stage form and the gate delay time per gate was measured at room temperature and at 77K. It was found that it was shortened about 0.7 to 0.5 time at 77K with respect to that obtained at room temperature.

LaB_6, TiN, ZrN, TaN and ZrC, which are materials easily fitted to the conventional silicon process were used.

In the MOSFET fabricated by using these materials, even after a high temperature accelerated deterioration test at aboult 175°C no variations in the flat band voltage of the MOS diode, the threshold voltage V_{th}^D of the FET and in the mutual conductance g_m were found. Further another high temperature accelerated deterioration test at about 175°C was effected also for a ring oscillator, in which the inverters described previously were connected in series, and neither variations in the threshold voltage V_{th} of the inverter nor deteriorations in the delay time at room temperature and 77K were observed after the test.

EMBODIMENT 1

A depletion type n channel MOSFET having the cross sectional structure as indicated in Figure 1 was fabricated by using LaB_6 for the gate electrode. LaB_6 was formed by the electron beam evaporation method. The LOCOS structure is used for the element isolation and the fabrication process is the well known self alignment type n MOS process. After the formation of the gate electrode As ions were implanted to form the source and the drain regions.

The impurity concentration in the p conductivity type Si substrate was about $1\times10^{16}cm^{-3}$; the gate oxide film was about 20mm thick; and the channel length was about 1μm. 6 sorts of MOSFETs were fabricated, in which the thickness of the gate electrode was at 6 levels, i.e. 20, 50, 100, 200, 500 and 1000mm.

Figure 2 is a graph showing results of measurements of the high frequency C-V curve of an MIS diode between the gate electrode 17 and the p conductivity type Si

substrate 7 for a frequency of about 1MHz at temperatures of 300K and 77K. The threshold voltage, at which the surface portion of the p conductivity type Si substrate ofthis MIS diode was inverted was about -1.6V. The C-V characteristics were not changed at room temperatureand 77K. Further the C-V characteristics indicated in Figure 2 do not depend on the thickness of the gate electrode.

The drain current (I_D) vs. gate voltage (V_G) characteristics of the fabricated MOSFET were those of the depletion type n channel MOSFET indicated in Figures 6(A) and 6(B) and the threshold voltage V_{th}^{D} of the MOSFET was about -1.6V at room temperature. The variation in the threshold voltage was smaller than 0.2V even at 77K. The current voltage characteristics of the MOSFET did not depend on the thickness of the gate electrode.

MOSFETs having various thicknesses of the gate oxide film and various impurity concentrations in the p conductivity type Si substrate were fabricated, the thickness of the gate electrode being kept constant at 500mm. The thickness of the gate oxide film were 5, 10, 20, 40, 60, 100, 120 and 140mm and the impurity concentrations in the substrate were $1x10^{15}$, $2x10^{15}$, $5x10^{15}$, $1x10^{16}$, $2x10^{16}$, $5x10^{16}$, $1x10^{17}$, $2x10^{17}$, $5x10^{17}$, $1x10^{18}$, $2x10^{18} cm^{-3}$, MOSFETs of all the possible combinations thereof being fabricated. Figure 3(A) shows the relation between the thickness T_{ox} of the gate oxide film, at which the threshold voltage is turned to a negative value, and the impurity concentration N_A of the p conductivity type Si substrate. when the thickness of the gate oxide film and the impurity concentration are in a region below the respective line (hatched region) in Figure 3(A), the threshold voltage was turned to be negative. In the case where the impurity concentration in the p conductivity type substrate was as small as $1x10^{15} cm^{-3}$ and the thickness of the gate oxide film was as small as 5mm, the lower limit of the threshold voltage was about -2V. The interfacial fixed charge density of the fabricated MOS diode described by

referring to Figures 2 and 3(A) in the present embodiment was 1 to $5x10^{10}cm^{-2}$.

EMBODIMENT 2

An inverter of E/D structure having the cross sectional structure as indicated in Figure 4, using LaB_6 for the gate electrode of the depletion type MOSFET and n^+ type polycrystalline silicon for the gate electrode of the enhancement type MOSFET and ring oscillator, in which inverters thus fabricated were connected in series, were fabricated. The channel length was 0.1μm or 0.5μm both for the depletion type and for the enhancement MOSFET. LaB_6 was formed by using the electron beam evaporation method and the n^+ type polycrystalline silcon was formed by the well known CVD method. The LOCOS structure is used for the element isolation and the fabrication process is the well known self alignment type n MOS process. After the formation of the gate electrode As ions were implanted to form the source and the drain regions. Ions were implanted in the channel position for the control of the threshold voltage. B ions were implanted in the channel portion of the enhancement MOSFET before the formation of the n^+ type polycrystalline silicon gate so that the threshold voltage of the enhancement MOSFET having a channel length of 0.5μm was about 0.7V and the threshold voltage of the enhancement type MOSFET having a channel length of 0.5μm was about 0.3V. On the other hand, B ions, which are impurities of same conductivity type as the p conductivity type Si substrate, are implanted in the channel position of the depletion type MOSFET before the formation of the LaB_6 gate so that the threshold voltage of the depletion type MOSFET having a channel length of 0.5μm was about -1.6V and the threshold voltage of the enhancement type MOSFET having a channel length of 0.1μm was about -1V.

Figures 5(A) and 6(A) show input voltage-output voltage characteristics of the inverter having the E/D structure using MOSFETs, whose channel lengths are 0.5μm and 0.1μm, respectively. The source voltage was 3.3V for the 0.5μm MOSFET and 1.5V for the 0.1μm MOSFET. The input-output voltage characteristics as indicated in Figures 5(A) and 6(A) were obtained both at room temperature and at 77K.

The gate delay time per gate of the ring oscillator was measured and it was found that at 77K, it was about 0.7 times as short as that obtained at room temperature.

EMBODIMENT 3

A depletion type MOSFET similar to that described in EMBODIMENT 1 was fabricated by replacing the gate electrode made of LaB_6 in EMBODIMENT 1 by TiN. TiN was formed by using the reactive sputtering method.

The obtained C-V characteristics and the current-voltage characteristics of the MOSFET were similar to those obtained in EMBODIMENT 1. Figure 3(B) shows the relation between the thickness of the gate oxide film, at which the threshold voltage is turned to a negative value, and the impurity concentration of the p conductivity type Si substrate. Similarly to that described in EMBODIMENT 1, when the thickness of the gate oxide film and the impurity concentration in the substrate are in a region below the respective line (hatched region) in Figure 3(B), the threshold voltage was turned to be negative. In the case where the impurity concentration in the p conductivity type substate was as small as $10^{15}cm^{-3}$ and the thickness of the gate oxide film was as small as 5mm, the lower limit of the threshold voltage was about -1.6V. The interfacial fixed charge density of the fabricated MOS diode described by referring to Figures 2 and 3(B) in the present embodiment was 1 to $5x10^{10}cm^{-2}$.

EMBODIMENT 4

An inverter of E/D structure having the cross sectional structure as indicated in Figure 4, by the process similar to that described in EMBODIMENT 2, using TiN for the gate electrode of the depletion type MOSFET and n^+ type polycrystalline silicon for the gate electrode of the enhancement type MOSFET and a ring oscillator, in which inverters thus fabricated were connected in series, were fabricated.

TiN was formed by using the reactive sputtering method and the n^+ type polycrystalline silicon was formed by the well known CVD method. Ions were implanted in the channel portion for the control of the threshold voltage similarly to EMBODIMENT 2.

Similarly to EMBODIMENT 2, for the MOSFETs having channel lengths of 0.5μm and 0.1μm the input voltage-output voltage characteristics of the inverters of E/D structure, as indicated in Figures 5(A) and 6(A) respectively, were obtained. The source voltage was 3.3V for the 0.5μm MOSFET and 1.5V for the 0.1μm MOSFET. The input-output voltage characteristics as indicated in Figures 5(A) and 6(A) were obtained both at the room temperature and at 77K.

The gate delay time per gate of the ring oscillator was measured and it was found that at 77K it was about 0.7 times as short as that obtained at room temperature.

EMBODIMENT 5

A depletion type MOSFET similar to that described in EMBODIMENT 1 was fabricated by replacing the gate electrode made of LaB_6 in EMBODIMENT 1 by ZrN. ZrN was formed by using the reactive sputtering method.

The obtained C-V characteristics and the current-voltage characteristics of the MOSFET were similar to those obtained in EMBODIMENT 1.

Figure 3(B) shows the relation between the thickness of the gate oxide film, at which the threshold voltage is turned to a negative value, and the impurity concentration of the p conductivity type Si substrate. Similarly to that described in EMBODIMENT 1, when the thickness of the gate oxide film and the impurity concentration are in a region below the respective line (hatched region) in Figure 3(B), the threshold voltage was turned to be negative. In the case where the impurity concentration in the p conductivity type substrate was as small as $10^{15}cm^{-3}$ and the thickness of the gate oxide film was as small as 5mm, the lower limit of the threshold voltage was about -2.4V. The interfacial fixed charge density of the fabricated MOS diode described by referring to Figures 2 and 3(B) in the present embodiment was 1 to $5x10^{10}cm^{-2}$.

EMBODIMENT 6

An inverter of E/D structure having the cross sectional structure as indicated in Figure 4, by the process similar to that described in EMBODIMENT 2, using ZrN for the gate electrode of the depletion type MOSFET and n^+ type polycrystalline silicon for the gate electrode of the enhancement type MOSFET and a ring oscillator, in which inverters thus fabricated were connected in series, were fabricated.

ZrN was formed by using the reactive sputtering method and the n^+ type polycrystalline silicon was formed by the well known CVD method. Ions were implanted in the channel position for the control of the threshold voltage, similarly to EMBODIMENT 2.

Similarly to EMBODIMENT 2, for the MOSFETs having channel lengths of $0.5\mu m$ and $0.1\mu m$ the input voltage-output voltage characteristics of the inverters of E/D structure, as indicated in Figures 5(A) and 6(A), respectively, were obtained. The source voltage was 3.3V

for the 0.5μm MOSFET and 1.5V for the 0.1μm MOSFET. The input-output voltage characteristics as indicated in Figures 5(A) and 6(A) were obtained both at room temperature and at 77K.

The gate delay time per gate of the ring oscillator was measured and it was found that at 77K it was about 0.7 times as short as that obtained at room temperature.

EMBODIMENT 7

An MOSFET was fabricated by replacing the gate metal LaB_6 in EMBODIMENT 1 by TaN. TaN was formed by using the reactive sputtering method.

The obtained C-V characteristics and the current-voltage characteristics of the MOSFET were similar to those obtained in EMBODIMENT 1. Figure 3(B) shows the relation between the thickness of the gate oxide film, at which the threshold voltage is turned to a negative value, and the impurity concentration of the p conductivity type Si substrate. Similarly to that described in EMBODIMENT 1 when the thickness of the gate oxide film and the impurity concentration in the substrate are in a region below the respective line (hatched region) in Figure 3(B), the threshold voltage was turned to be negative. In the case where the impurity concentration in the p conductivity type substrate was so small as $10^{15}cm^{-3}$ and the thickness of the gate oxide film was as small as 5mm, the lower limit of the threshold voltage was about -2.4V. The interfacial fixed charge density of the fabricated MOS diode described by referring to Figures 2 and 3(B) in the present embodiment was 1 to $5x10^{10}cm^{-2}$.

EMBODIMENT 8

An inverter of E/D structure having the cross sectional structure as indicated in Figure 4, by the process similar to that described in EMBODIMENT 2, using

TaN for the gate electrode of the depletion type MOSFET and n^+ type polycrystalline silicon for the gate electrode of the enhancement type MOSFET and a ring oscillator, in which inverters thus fabricated were connected in series, were fabricated.

TaN was formed by using the reactive sputtering method and the n^+ type polycrystalline silicon was formed by the well known CVD method. Ions were implanted in the channel portion for the control of the threshold voltage, similarly to EMBODIMENT 2.

Similarly to EMBODIMENT 2, for the MOSFETs having channel lengths of 0.5μm and 0.1μm the input voltage-output voltage characteritics of the inverters of E/D structure as indicated in Figures 5(A) and 6(A) respectively were obtained. The source voltage was 3.3V for the 0.5μm MOSFET and 1.5V for the 0.1μm MOSFET. The input-output voltage characteristics as indicated in Figures 5(A) and 6(A) were obtained both at room temperature and at 77K.

The gate delay time per gate of the ring oscillator was measured and it was found that at 77K it was about 0.7 times as short as that obtained at room temperature.

EMBODIMENT 9

A depletion type MOSFET similar to that described in EMBODIMENT 1 was fabricated by replacing the gate electrode made of LaB_6 in EMBODIMENT 1 by ZrC. ZrC was formed by using the reactive sputtering method.

The obtained C-V characteristics and the current-voltage characteristics of the MOSFET were simlar to those obtained in EMBODIMENT 1.

Figure 3(B) shows the relation between the thickness of the gate oxide film, at which the threshold voltage is turned to a negative value, and the impurity concentration of the p conductivity type Si substrate. Similarly to that described in EMBODIMENT 1, when the

thickness of the gate oxide film and the impurity concentration are in a region below the respective line (hatched region) in Figure 3(B), the threshold voltage was turned to be negative. In the case where the impurity concentration in the p conductivity type substrate was as small as $10^{15}cm^{-3}$ and the thickness of the gate oxide film was as small as 5mm, the lower limit of the threshold voltage was about -2.4V. The interfacial fixed charge density of the fabricated MOS diode described by referring to Figures 2 and 3(B) in the present embodiment was 1 to $5x10^{10}cm^{-2}$.

EMBODIMENT 10

An inverter of E/D structure having the cross sectional structure as indicated in Figure 4, by the process similar to that described in EMBODIMENT 2, using ZrC for the gate electrode of the depletion type MOSFET and n^+ type polycrystalline silicon for the gateelectrode of the enhancement type MOSFET and a ring oscillator, in which inverters thus fabricated were connected in series, were fabricated.

ZrC was formed by using the reactive sputtering method and the n^+ type polycrystalline silicon was formed by the well known CVD method. Ions were implanted in the channel portion for the control of the threshold voltage, similarly to EMBODIMENT 2.

Similarly to EMBODIMENT 2, for the MOSFETs having channel lengths between 0.5μm and 0.1μm the input voltage-output voltage characteristics of the inverters of E/D structure, as indicated in Figures 5(A) and 6(A), respectively, were obtained. The source voltage was 3.3V for the 0.5μm MOSFET and 1.5V for the 0.1μm MOSFET. The input-output voltage characteristics as indicated in Figures 5(A) and 6(A) were obtained both at room temperature and at 77K.

The gate delay time per gate of the ring oscillator was measured and it was found that at 77K it was about 0.7 times as short as that obtained at room temperature.

EMBODIMENT 11

In EMBODIMENTs 1 and 2, the gate electrode of the depletion type MOSFET was of one-layered structure made of LaB_6. A depletion type MOSFET having a gate of two-layered structure was fabricated by forming a W or Mo or titanium silicide or wolfram silicide film after the formation of the gate electrode made of LaB_6. The film made of W or Mo or titanium silicide or wolfram silicide on the LaB_6 layer was 800mm thick. MOSFETs having the LaB_6 layer of various levels of the thickness of 10, 20, 50 and 10mm were fabricated. The W or Mo or titanium silicide or wolfram silicide film was formed by the well known sputtering method.

The MOS diode characteristics, the characteristics of the depletion type MOSFET, the result indicated in Figure 3(B), the characteristics of the inverter and the characteristics of the ring oscillator, which are obtained were identical to those described in EMBODIMENTs 1 and 2, independently of the W or Mo or titanium silicide or wolfram silicide film formed on the LaB_6 layer.

EMBODIMENT 12

In EMBODIMENTS 3 and 4, the gate electrode of the depletion type MOSFET was of one-layered structure made of TiN. A depletion type MOSFET having a gate of two-layered structure was fabricated by forming a W or Mo or titanium silicide or wolfram silicide film after the formation of the gate electrode made of TiN. The film made of W or Mo or titanium silicide film on the TiN layer was 800mm thick. MOSFETs having the TiN layer of various levels of the thickness of 10, 20, 50 and 100mm

were fabricated. The W or Mo or titanium silicide or wolfram silicide film was formed by the well known sputtering method.

The MOS diode characteristics, the characteristics of the depletion type MOSFET, the result indicated in Figure 3(B), the characteristics of the inverter and the characteristics of the ring oscillator, which are obtained were identical to those described in EMBODIMENTs 3 and 4, independently of the W or Mo or titanium silicide or wolfram silicide film formed on the TiN layer.

EMBODIMENT 13

In EMBODIMENTS 5 and 6, the gate electrode of the depletion type MOSFET was of one-layered structure made of ZrN. A depletion type MOSFET having a gate of two-layered structure was fabricated by forming a W or Mo or titanium silicide or wolfram silicide film after the formation of the gate electrode made of ZrN. The film made of W or Mo or titanium silicide or wolfram silicide film on the ZrN layer was 800mm thick. MOSFETs having the ZrN layer of various levels of the thickness of 10, 20, 50 and 100mm were fabricated. The W or Mo or titanium silicide or wolfram silicide film was formed by the well known sputtering method.

The MOS diode characteristics, the characteristics of the depletion type MOSFET, the result indicated in Figure 3(B), the characteristics of the inverter and the characteristics of the ring oscillator, which are obtained were identical to those described in EMBODIMENTs 3 and 4, independently of the W or Mo or titanium silicide or wolfram silicide film formed on the ZrN layer.

EMBODIMENT 14

In EMBODIMENTs 7 and 9, the gate electrode of the depletion type MOSFET was of one-layered structure made of

TaN. A depletion type MOSFET having a gate of two-layered structure was fabricated by forming a W or Mo or titanium silicide or wolfram silicide film after the formation of the gate electrode made of TaN. The film made of W or Mo or titanium silicide or wolfram silicide film on the TaN layer was 800mm thick. MOSFETs having the TaN layer of various levels of the thickness of 10, 20, 50 and 100mm were fabricated. The W or Mo or titanium silicide or wolfram silicide film was formed by the well known sputtering method.

The MOS diode characteristics, the characteristics of the depletion type MOSFET, the result indicated in Figure 3(B), the characteristics of the inverter and the characteristics of the ring oscillator, which are obtained were identical to those described in EMBODIMENTs 5 and 6, independently of the W or Mo or titanium silicide or wolfram silicide film formed on the TaN layer.

EMBODIMENT 15

In EMBODIMENTs 7 and 8, the gate electrode of the depletion type MOSFET was of one-layered structure made of ZrC. A depletion type MOSFET having a gate of two-layered structure was fabricated by forming a W or Mo or titanium silicide or wolfram silicide film after the formation of the gate electrode made of ZrC. The film made of W or Mo or titanium silicide or wolfram silicide film on the ZrC layer was 800mm thick. MOSFETs having the ZrC layer of various levels of the thickness of 10, 20, 50 and 100mm were fabricated. The W or Mo or titanium silicide or wolfram silicide film was formed by the well known sputtering method.

The MOS diode characteristics, the characteristics of the depletion type MOSFET, the result indicated in Figure 3(B), the characteristics of the inverter and the characteristics of the ring oscillator, which are obtained were identical to those described in EMBODIMENTs 7 and 8,

independently of the W or Mo or titanium silicide or wolfram silicide film formed on the ZrC layer.

EMBODIMENT 16

The gate metal of the depletion type MOSFET in the inverter of E/D structure and the ring oscillator described in EMBODIMENTs 2 and 11 was of one-layered structure made of LaB_6 or two-layered structure made of LaB_6 and another material (W or Mo or titanium silicide or wolfram silicide). On the other hand, the gate metal of the enhancement type MOSFET was made of n^+ type polycrystalline Si in all the cases.

Inverters of E/D structure and ring oscillators were fabricated by using W or Mo or titanium silicide or wolfram silicide for the gate metal of the enhancement type MOSFET described in EMBODIMENTs 2 and 11. W or Mo or titanium silicide or wolfram silicide was formed by the well known sputtering method.

Results similar to those described in EMBODIMENTS 2 and 11 were obtained for the characteristics of the inverters and the characteristics of the ring oscillators which were obtained independently of the sort of the gate metal of the enhancement type MOSFET.

EMBODIMENT 17

The gate metal of the depletion type MOSFET in the inverter of E/D structure and the ring oscillator described in EMBODIMENTs 4 and 12 was of one-layered structure made of TiN or two-layered structure made of TiN and another material (W or Mo or titanium silicide or wolfram silicide). On the other hand, the gate metal of the enhancement type MOSFET was made of n^+ type polycrystalline Si in all the cases.

Inverters of E/D structure and ring oscillators were fabricated by using W or Mo or titanium silicide or

wolfram silicide for the gate metal of the enhancement type MOSFET described in EMBODIMENTs 4 and 12. W or Mo or titanium silicide or wolfram silicide was formed by the well known sputtering method.

Results similar to those described in EMBODIMENTS 4 and 12 were obtained for the characteristics of the inverters and the characteristics of the ring oscillators which were obtained independently of the sort of the gate metal of the enhancement type MOSFET.

EMBODIMENT 18

The gate metal of the depletion type MOSFET in the inverter of E/D structure and the ring oscillator described in EMBODIMENTs 6 and 13 was of one-layered structure made of ZrN or two-layered structure made of ZrN and another material (W or Mo or titanium silicide or wolfram silicide). On the other hand, the gate metal of the enhancement type MOSFET was made of n^+ type polycrystalline Si in all the cases.

Inverters of E/D structure and ring oscillators were fabricated by using W or Mo or titanium silicide or wolfram silicide for the gate metal of the enhancement type MOSFET described in EMBODIMENTs 6 and 13. W or Mo or titanium silicide or wolfram silicide was formed by the well known sputtering method.

Results similar to those described in EMBODIMENTS 6 and 13 were obtained for the characteristics of the inverters and the characteristics of the ring oscillators which were obtained independently of the sort of the gate metal of the enhancement type MOSFET.

EMBODIMENT 19

The gate metal of the depletion type MOSFET in the inverter of E/D structure and the ring oscillator described in EMBODIMENTs 8 and 14 was of one-layered

structure made of TaN or two-layered structure made of TaN and another material (W or Mo or titanium silicide orwolfram silicide). On the other hand, the gate metal of the enhancement type MOSFET was made of n^+ type polycrystalline Si in all the cases.

Inverters of E/D structure and ring oscillators were fabricated by using W or Mo or titanium silicide or wolfram silicide for the gate metal of the enhancement type MOSFET described in EMBODIMENTs 8 and 14. W or Mo or titanium silicide or wolfram silicide was formed by the well known sputtering method.

Results similar to those described in EMBODIMENTS 8 and 14 were obtained for the characteristics of the inverters and the characteristics of the ring oscillators which were obtained independently of the sort of the gate metal of the enhancement type MOSFET.

EMBODIMENT 20

The gate metal of the depletion type MOSFET in the inverter of E/D structure and the ring oscillator described in EMBODIMENTs 10 and 15 was of one-layered structure made of ZrC or two-layered structure made of ZrC and another material (W or Mo or titanium silicide or wolfram silicide). On the other hand, the gate metal of the enhancement type MOSFET was made of n^+ type polycrystalline Si in all the cases.

Inverters of E/D structure and ring oscillators were fabricated by using W or Mo or titanium silicide or wolfram silicide for the gate metal of the enhancement type MOSFET described in EMBODIMENTs 10 and 15. W or Mo or titanium silicide or wolfram silicide was formed by the well known sputtering method.

Results similar to those described in EMBODIMENTS 10 and 15 were obtained for the characteristics of the inverters and the characteristics of the ring oscillators which were obtained independently of the sort of the gate metal of the enhancement type MOSFET.

EMBODIMENT 21

Although in the above embodiments p conductivity type Si was used for the substrate, also in the case wherein conductivity type Si was used, it was possible to fabricate a depletion type p channel MOSFET and an inverter of E/D structure without doping the channel portion of the depletion type MOSFET with B atoms, which are impurities of conductivity type opposite to n conductivity type Si. Although Se, Ir, Pt, etc., which are substances whose work function is greater than about 5.5V, among substances whose work function is greater than that of the n conductivity type Si, can be used for the gate electrode of the depletion type p channel MOSFET, it is desirable to use Pt therefor, which can be formed easily by the electron beam evaporation method, etc. and which has a melting point of about 1770°C. It was possible to obtain a depletion type MOSFET and a p channel inverter of E/D structure performing the depletion operation both at room temperature and at low temperature by using platinum for the gate electrode.

The depletion type MOSFET can be operated both at room temperature and at liquid nitrogen temperature and the inverter of E/D structure can be operated also both at room temperature and at liquid nitrogen temperature.

The MOSFET integrated circuit using depletion type MOSFETs and inverters of E/D structure can provide a high speed and high density integrated circuit having the high speed of an integrated circuit using bipolar transistors and a high degree of integration of MOSFETs together by driving it at liquid nitrogen temperature.

Further the inverter of E/D structure can provide a high speed and high density integrated circuit with a simple fabrication process and a small number of MOSFETs, differently from the inverter of CMOS structure.

Furthermore, since the MOSFET integrated circuit can be operated both at room temperature and at liquid nitrogen temperature, it is possible at constructing a system to check the operation at room temperature, to exchange defective chips on boards, to verify the normal operation of the system, and thereafter to drive the system with the highest operational performance at liquid nitrogen temperature.

In addition, if LaB_6, TiN, ZiN, TaN or ZrC is used for the gate electrode, it is possible to provide an integrated circuit having a high reliability which has a high adaptability to the conventional Si process and gives rise to no variations in characteristics even by the accelerated deterioration test.

CLAIMS

1. An integrated circuit including a depletion type field effect transistor comprising a first conductivity type semiconductor substrate; a source region formed on the principal surface side of said semiconductor substrate; a drain region formed in the neighbourhood of said source region on the principal surface side of said semiconductor substrate; a gate insulating film formed on the surface portion of said semiconductor substrate between said source region and said drain region which portion is not doped with an impurity of second conductivity type opposite to the first conductivity type; and a gate electrode formed on said gate insulating film comprising at least a layer of one of a group of materials comprising a nitride, a carbide and LaB_6 having a work function smaller than that of said first conductivity type semiconductor substrate and a further layer of one of a group of materials comprising polycrystalline silicon, a high melting point metal or silicide on any said layer of LaB_6.

2. An integrated circuit according to Claim 1, wherein said gate electrode comprises a layer of a nitride or a carbide formed on said gate insulating film and a further layer of one of a group of materials comprising polycrystalline silicon, a high melting point metal and a silicide.

3. An integrated circuit according to Claim 1, wherein said gate electrode is formed from a single layer of one of a group of materials comprising TiN, ZrN, TaN, and ZrC.

4. An integrated circuit according to Claim 1, Claim 2 or Claim 3, wherein said surface portion of said semiconductor substrate between said source region and said drain region, which is not doped with first

conductivity type impurities, is not doped with impurities of same conductivity type as said semiconductor substrate.

5. An integrated circuit including at least one E/D inverter comprising a first conductivity type semiconductor substrate; a source region of an enhancement type MOSFET and a drain region of a depletion type MOSFET formed with a distance on the principal surface side of said semiconductor substrate; an island-shaped common region acting as a drain region of said enhancement type MOSFET and a source region of said depletion type MOSFET between said source region of said enhancement type MOSFET and said drain region of said depletion type MOSFET; a gate insulating film for said depletion type MOSFET formed on the surface portion of said semiconductor substrate between said drain region of said depletion type MOSFET and said common region, which portion is not doped with impurities of conductivity type, which is opposite to the conductivity type of said semiconductor substrate; a gate electrode for said depletion type MOSFET formed on said gate insulated film for said depletion type MOSFET comprising at least a layer of one of a group of materials comprising a nitride, a carbide and LaB_6 and a further layer of one of a group of materials comprising polycrystalline silicon, a high melting point metal or silicide on any said layer of LaB_6; an electrode formed on said common region and connected electrically with said gate electrode for said depletion type MOSFET; a gate insulating film for said enhancement type MOSFET formed on the surface portion of said semiconductor substrate between said source region of said enhancement type MOSFET and said common region, which portion is doped with impurities of conductivity type, which is the same as the conductivity type of said semiconductor substrate;and a gate electrode for said enhancement type MOSFET formed on said gate insulated film for said enhancement type MOSFET.

6. An integrated circuit according to Claim 5, wherein said gate electrode for said depletion type MOSFET comprises a layer of a nitride or a carbide formed on said gate insulating film and a further layer of one of a group of materials comprising polycrystalline silicon, a high melting point metal and a silicide.

7. An integrated circuit according to Claim 5, wherein said gate electrode for said depletion type MOSFET comprises a single layer of one of a group of materials comprising TiN, ZiN, TaN and ZrC.

8. An integrated circuit according to Claims 5, 6 or 7, wherein said gate electrode for said enhancement type MOSFET comprises one of a group of materials comprising polycrystalline silicon, high melting point metal, a silicide and aluminium.

9. An integrated circuit according to Claims 5, 6 or 7, wherein said gate electrode for said enhancement type MOSFET comprises a layer of polycrystalline silicon formed on said gate insulating film for said enhancement type MOSFET and a layer of a silicide formed on said polycrystalline silicon layer.

10. An integrated circuit according to any preceding claim, wherein the distance between said source region and said drain region formed on the surface of said semiconductor substrate is smaller than 0.5μm.

11. An integrated circuit according to any of Claims 1 to 4, wherein the source-drain voltage for said single depletion type field effect transistor, or the voltage supplied to said semiconductor integrated circuit is below 5V DC.

12. An integrated circuit according to any of Claims 5 to 10, wherein the source-drain voltage for the voltage between the ground of said enhancement/depletion type inverter and said drain of said depletion type field effect transistor, or the voltage to said semiconductor integrated circuit is below 5V DC.

13. An integrated circuit as hereinbefore described with reference to Figures 1 to 6 and 13 of the drawings.

Published 1991 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.

Family list
19 family members for: **GB2243948**
Derived from 11 applications

1 INTEGRATED CIRCUIT
Inventor: MIKOSHIBA NOBUO (JP); TSUBOUCHI KAZUO (JP); (+1)
Applicant: MIKOSHIBA NOBUO (JP); TSUBOCHI KAZUO (JP); (+1)
EC: H01L27/088D; H01L29/49; (+3)
IPC: ***H01L29/78; H01L21/8236; H01L27/088*** (+6)
Publication info: CA2014296 A1 - 1990-10-21
CA2014296 C - 2000-08-01

2 INTEGRATED CIRCUIT
Inventor: MIKOSHIBA NOBUO (JP); TSUBOUCHI KAZUO (JP); (+1)
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EC: H01L27/088D; H01L29/49; (+3)
IPC: ***H01L27/088; H01L29/49***; **H01L27/085** (+2)
Publication info: CA2027528 A1 - 1991-10-21
CA2027528 C - 2000-09-05

3 INTEGRIERTE SCHALTUNGSANORDUNG
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IPC: ***H01L29/78; H01L21/8236; H01L27/088*** (+7)
Publication info: DE4012681 A1 - 1990-10-25

4 Construction of MOS integrated circuit for use at low temperature - has depletion transistors with gate-electrode which has low work function and enhancement devices using high work function material
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IPC: ***H01L27/088; H01L29/49***; **H01L27/085** (+3)
Publication info: DE4033141 A1 - 1991-10-24

5 CIRCUIT INTEGRE DU TYPE MOSFET, EN PARTICULIER INVERSEUR LOGIQUE
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EC: H01L27/088D; H01L29/49; (+3)
IPC: ***H01L29/78; H01L21/8236; H01L27/088*** (+7)
Publication info: FR2646289 A1 - 1990-10-26
FR2646289 B1 - 1994-08-19

6 Field effect transistor
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IPC: ***H01L27/088; H01L29/49***; **H01L27/085** (+4)
Publication info: FR2661277 A1 - 1991-10-25
FR2661277 B1 - 1993-03-12

7 Field effect transistor
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IPC: ***H01L29/78; H01L21/8236; H01L27/088*** (+6)
Publication info: GB2231720 A - 1990-11-21
GB2231720 B - 1993-08-11
GB9008525D D0 - 1990-06-13

8 Field effect transistor
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IPC: ***H01L27/088; H01L29/49***; **H01L27/085** (+2)
Publication info: GB2243948 A - 1991-11-13
GB2243948 B - 1994-06-08
GB9021721D D0 - 1990-11-21

9 INTEGRATED CIRCUIT
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IPC: ***H01L29/78; H01L21/8236; H01L27/088***

(+7)

Publication info: JP3048460 A - 1991-03-01

10 **CIRCUIT INTEGRE DU TYPE MOSFET, EN PARTICULIER INVERSEUR LOGIQUE**

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IPC: ***H01L29/78; H01L21/8236; H01L27/088*** (+6)

Publication info: NL9000949 A - 1990-11-16

11 **Integrated circuit**

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IPC: ***H01L27/088; H01L29/49***; **H01L27/085** (+3)

Publication info: US5245207 A - 1993-09-14